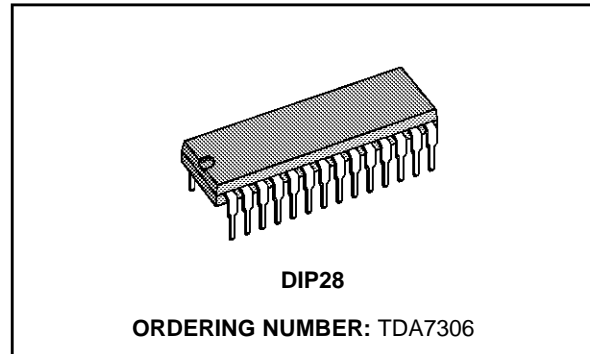


**DIGITAL CONTROLLED STEREO AUDIO PROCESSOR**

ADVANCE DATA

- CONTROL IS ACCOMPLISHED BY MICROWIRE/SPI - COMPATIBLE SERIAL BUS INTERFACE
- INPUT AND OUTPUT PINS FOR EXTERNAL EQUALIZER
- THREE STEREO INPUT SOURCE SELECTION PLUS MONO INPUT
- TREBLE, BASS, VOLUME AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (FRONT/REAR)
- SINGLE SUPPLY OPERATION
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING



balance (left/right) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi systems.

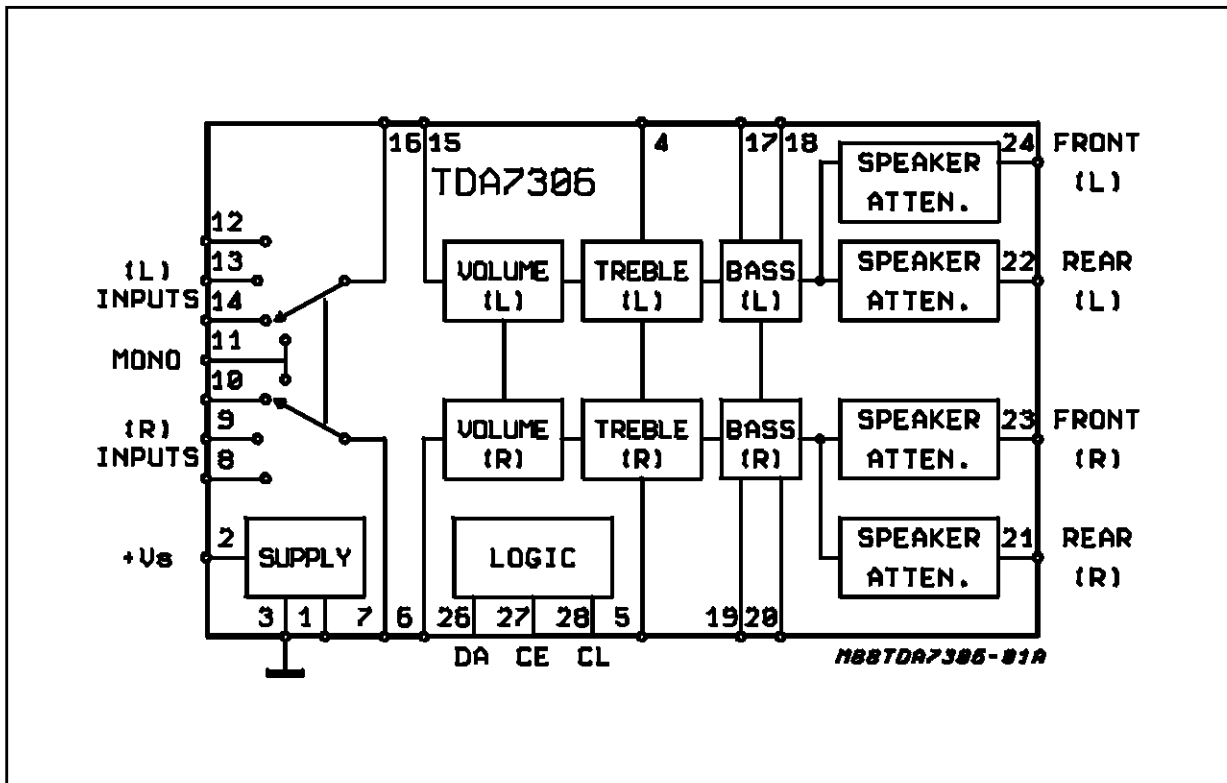
The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers.

The results are: low noise, low distortion and high dynamic range.

**DESCRIPTION**

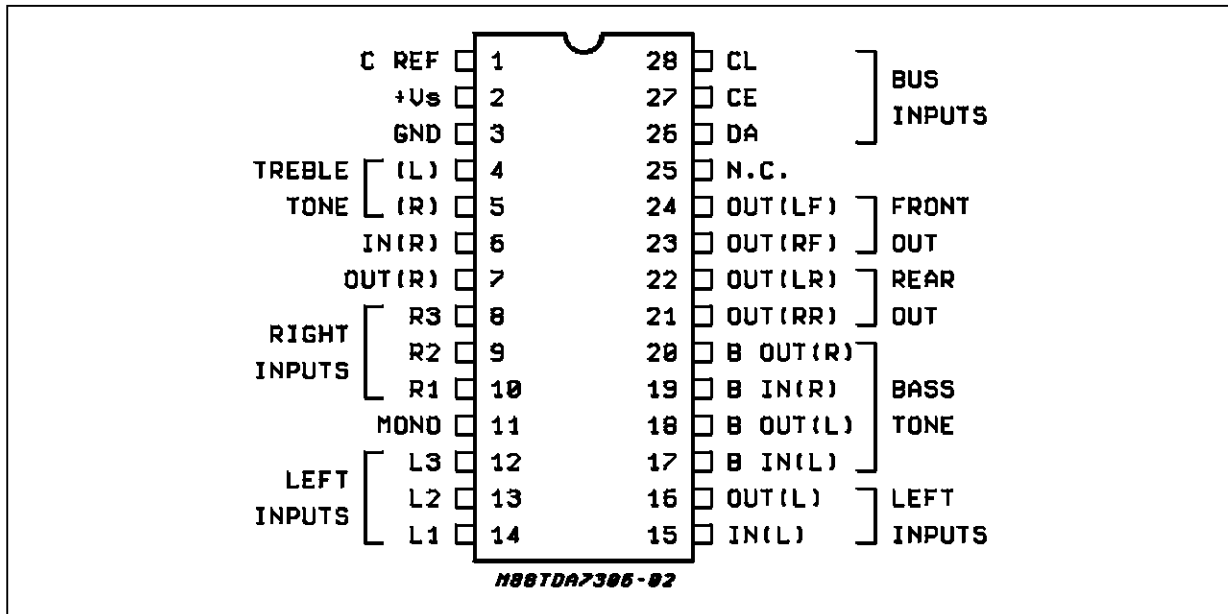
The TDA7306 is a volume, tone (bass and treble),

**BLOCK DIAGRAM**



# TDA7306

## PIN CONNECTION (Top view)



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_S$	Supply Voltage	14	V
$P_{tot}$	Total Power Dissipation ( $T_{amb} = 25^\circ\text{C}$ )	2	W
$T_{amb}$	Operating Ambient Temperature Range	-40 to +85	$^\circ\text{C}$
$T_{stg}$	Storage Temperature	-40 to 150	$^\circ\text{C}$

## THERMAL DATA

Symbol	Description	Value	Unit
$R_{th\ j-pins}$	Thermal Resistance Junction-pins	Max 65	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^\circ\text{C}$ ,  $V_S = 10\text{V}$ ,  $R_L = 10\text{K}\Omega$ ;  $R_g = 600\Omega$ ,  $f = 1\text{KHz}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

### SUPPLY

$V_S$	Supply Voltage		6	10	14	V
$I_S$	Supply Current		15	30	40	mA
SVR	Ripple Rejection	$f = 300\text{Hz to } 10\text{KHz}$	50	60		dB

### INPUT SELECTORS

$R_i$	Input Resistance		30	45		$\text{K}\Omega$
$V_i(\text{DC})$	Input DC Voltage		3.5	4.3	5	V
$V_{IN\ MAX}$	Max. Input Signal	$GV = 0\text{dB}$ $d = 0.3\%$	1.5	2.0		$V_{rms}$
$IN_S$	Input Separation	$f = 1\text{KHz}$ (2)	90	100		dB
		$f = 10\text{KHz}$ (2)	70	80		dB
$R_L$	Output Load Resistance		5			$\text{K}\Omega$

**ELECTRICAL CHARACTERISTICS** (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

**VOLUME CONTROLS**

$R_{IN}$	Input Resistance		10	18	26	K $\Omega$
	Control Range			78		dB
$G_{max}$	Max Gain		8	10	12	dB
	Max Attenuation		48	52.4		dB
	Step Resolution			1.6	2.5	dB
	Attenuator Set Error	$G_V = -50$ to 10dB			2	dB
	Tracking Error				2	dB

**SPEAKER ATTENUATORS**

	Control Range		38	41	44	dB
	Step Resolution	see Note (3)				
	Attenuator Set Error				3	dB
	Tracking Error				2	dB

**BASS AND TREBLE CONTROL (1)**

	Control Range			$\pm 15$		dB
	Step Resolution			2.5	3.5	dB

**AUDIO OUTPUT**

$V_O$	Max. Output Voltage	$d = 0.3\%$	1.5	2.2		V <sub>rms</sub>
$R_L$	Output Load Resistance		2			K $\Omega$
$C_L$	Output Load Capacitance				1	nF
$R_O$	Output Resistance			70	150	$\Omega$
$V_O(DC)$	DC Voltage Level		3	3.8	4.5	V

**GENERAL**

$e_{NO}$	Output Noise	BW = 22Hz to 22KHz	$G_V = 0$ dB Out atten. $\geq 20$ dB		6 3.5	15	$\mu$ V
		$G_V = 0$ dB	Curve A		4		
S/N	Signal to Noise Ratio	All gain = 0dB $V_O = 1$ V <sub>rms</sub> BW = 22Hz to 22KHz			105		dB
d	Distortion	f = 1KHz; $V_O = 1$ V; $G_V = 0$			0.01	0.1	%
	Frequency Response (-1dB)	$G_V = 0$	High Low	20		20	KHz Hz
$S_C$	Channel Separation left/right	f = 1KHz f = 10KHz		90 70	100 80		dB dB

**BUS INPUTS**

$V_{IL}$	Input LOW Voltage				0.8	V
$V_{IH}$	Input HIGH Voltage		2.4			V
	Digital Input Current		-5		+5	$\mu$ A

**Notes:**

- (1) Bass and Treble response see attached diagram. The center frequency and quality of the resonance behaviour can be chosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.
- (2) The selected input is grounded thru the 2.2 $\mu$ F capacitor.
- (3) See speaker attenuators table on "Software specification".

TDA7306

Figure 1: Application Circuit

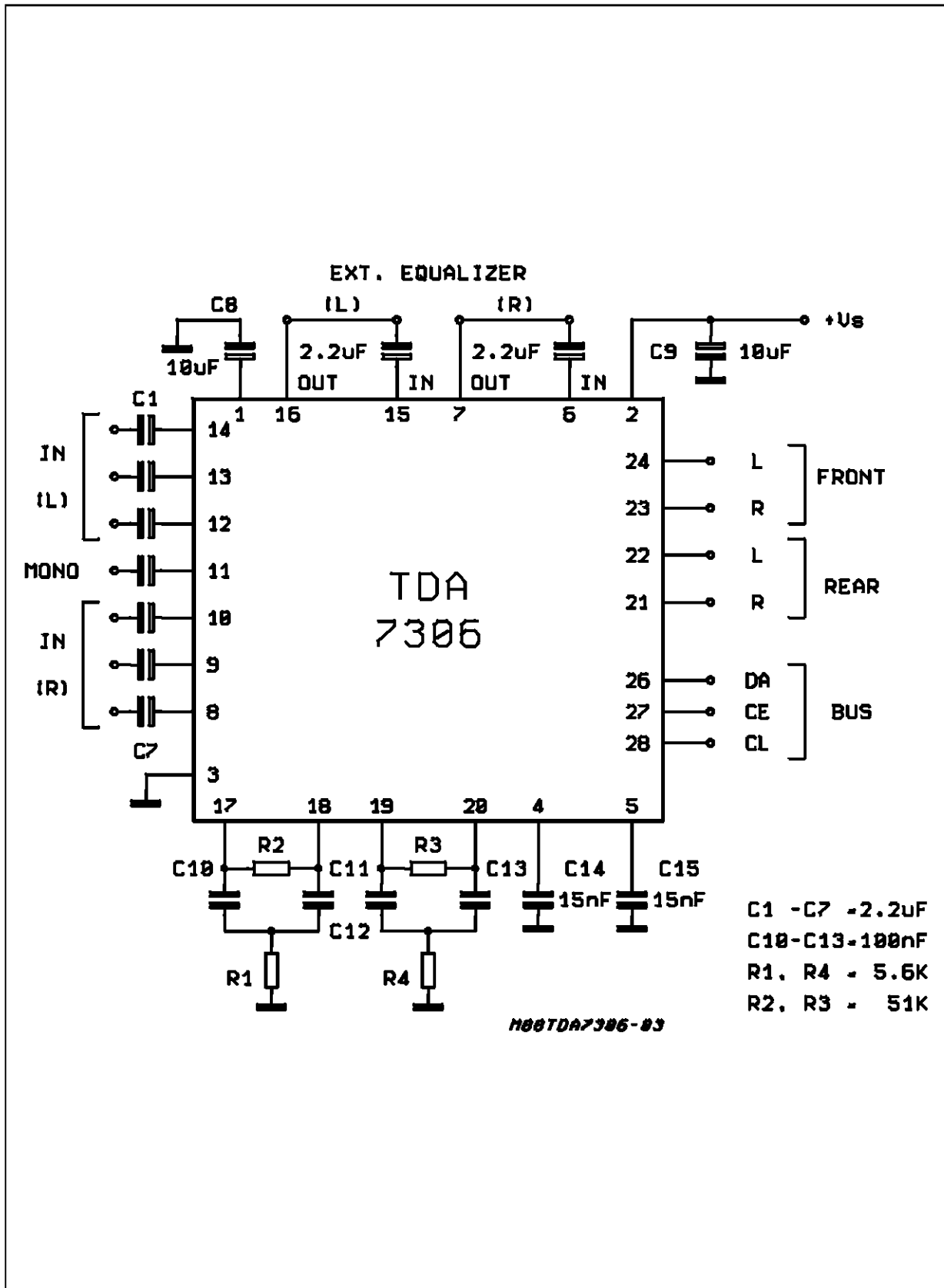


Figure 2: P.C. Board and Components Layout of the Fig.1 (1:1 scale)

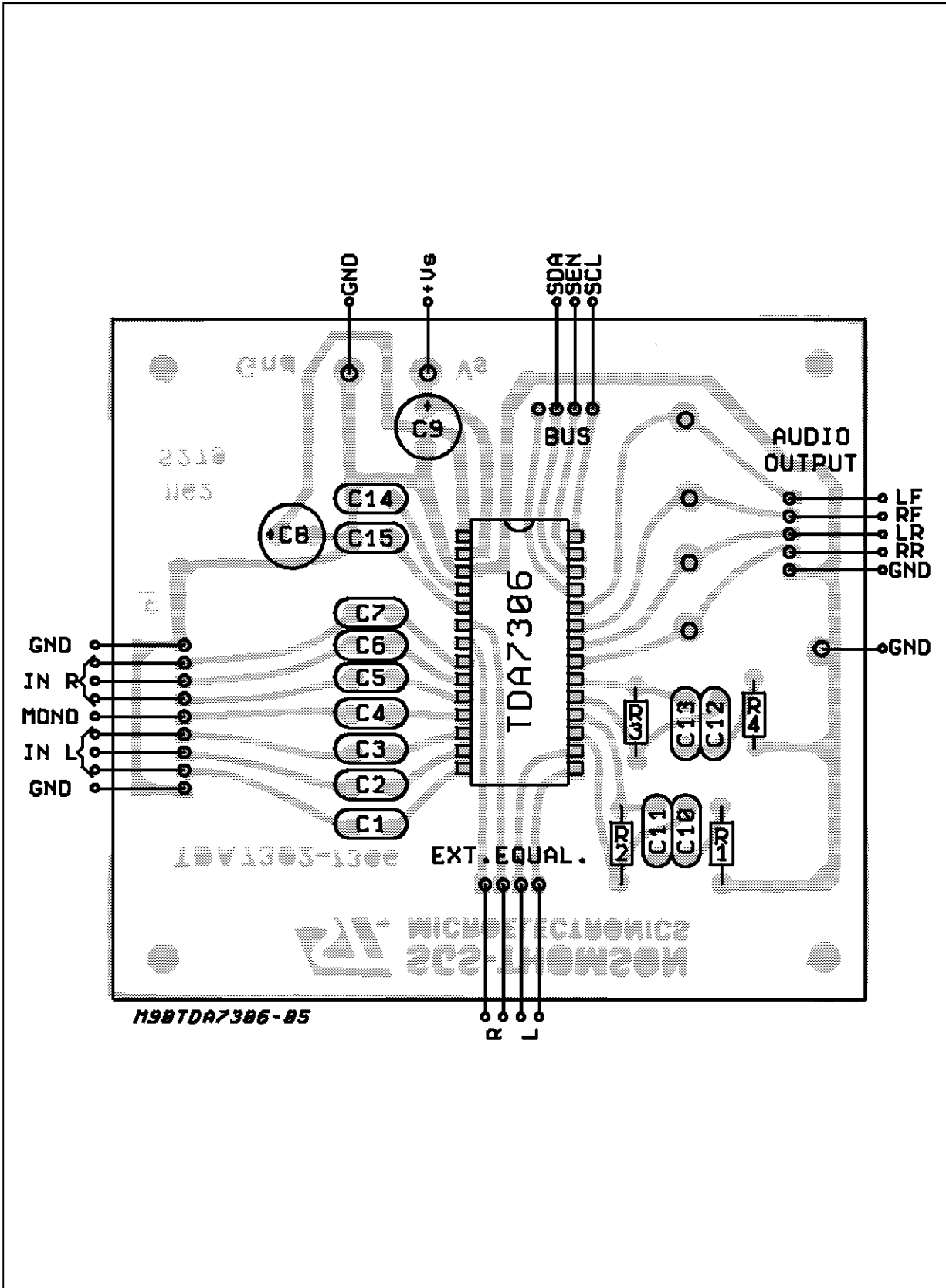


Figure 3: Total Output Noise vs. Volume Setting

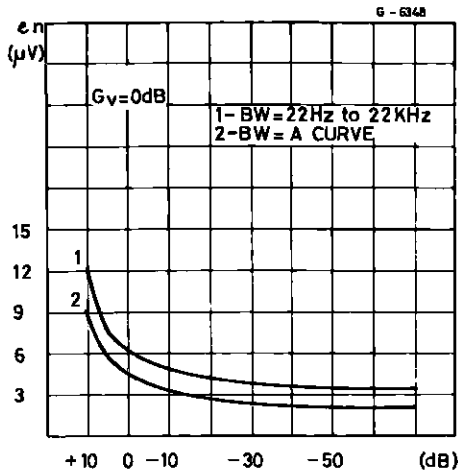


Figure 4: Signal to Noise Ratio vs. Volume Setting

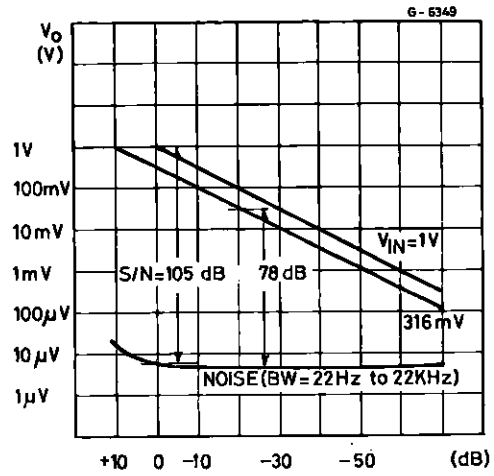


Figure 5: Distortion + Noise vs. Frequency

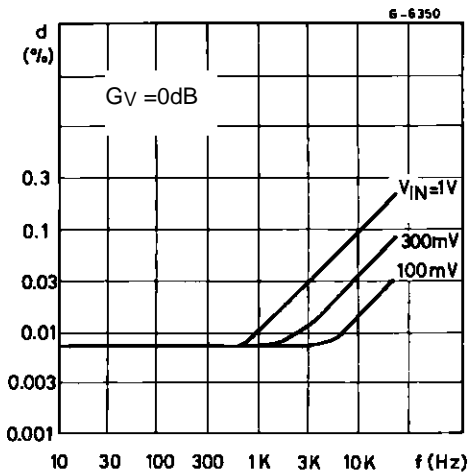


Figure 6: Distortion vs. Output Voltage

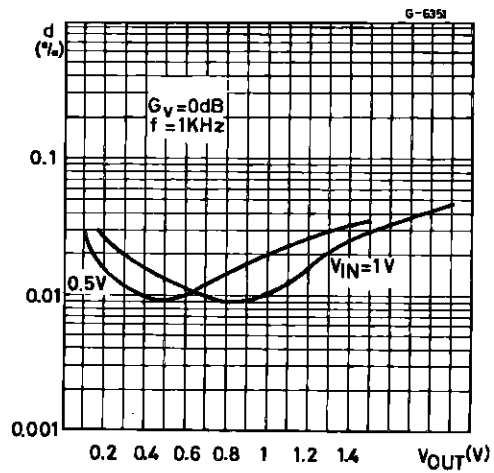


Figure 7: Distortion vs. Load Resistance

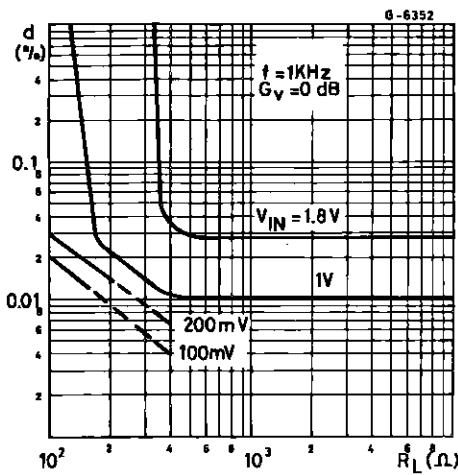


Figure 8: Channel Separation (L1 - R1) vs. Frequency

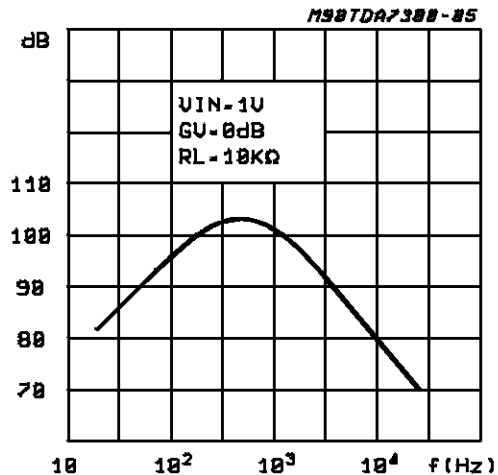


Figure 9: Input Separation (L1 - L2) vs. Frequency

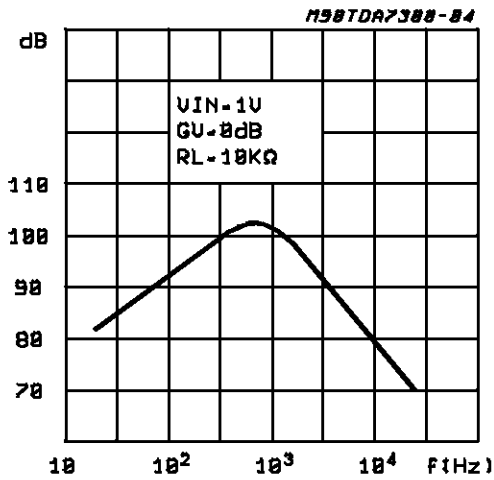


Figure 10: Supply Voltage Rejection vs. Frequency

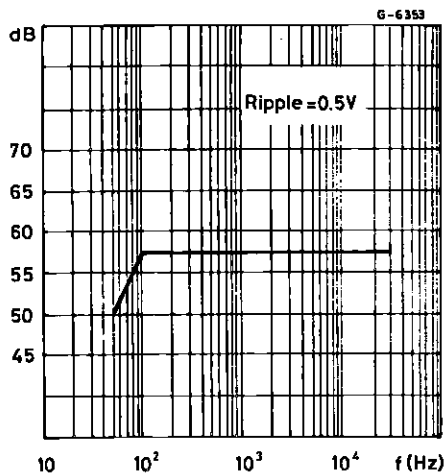
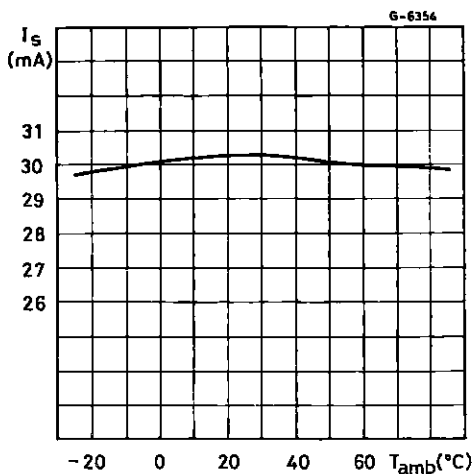


Figure 11: Quiescent Current vs. Temperature



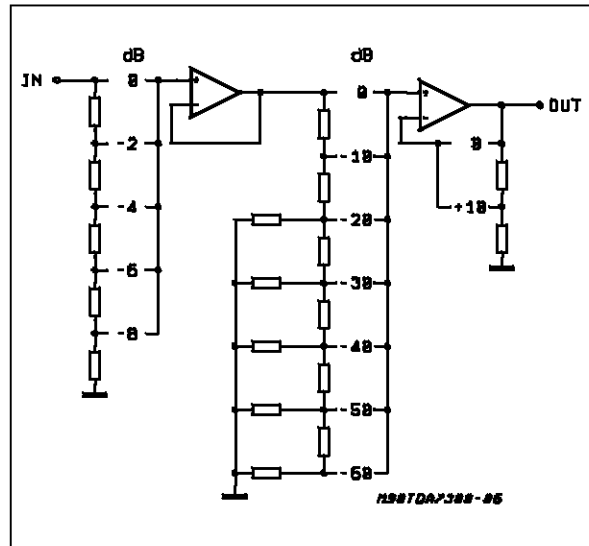
**APPLICATION INFORMATION**

**Volume Control Concept**

Traditional electronic volume control circuits use a multiplier technique with all the disadvantages of high noise and distortion.

The used concept, as shown in Fig. 12 with digital switched resistor dividers, provides extremely low noise and distortion. The multiplexing of the resistive dividers is realized with a multiple-input operational amplifier.

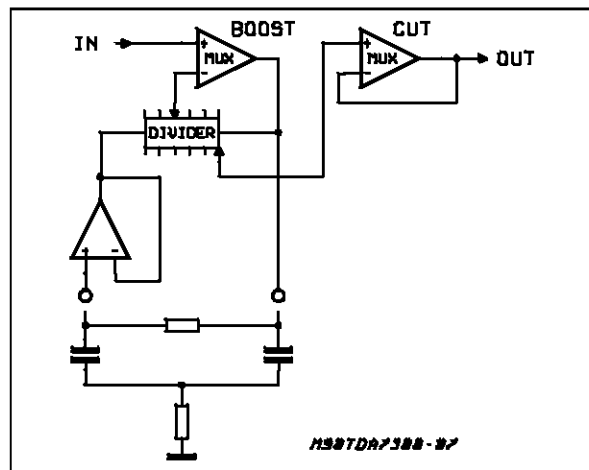
Figure 12: Volume Control



**Bass and Treble Control**

The principle operation of the bass control is shown in Fig. 13. The external filter together with the internal buffer allows a flexible filter design according to the different requirements in car radios. The function of the treble is similar to the bass. A typical curve is shown in Fig. 14.

Figure 13: Bass Control



APPLICATION INFORMATION (continued)

Outputs

A special class-A output amplifier with a modu-

lated sink current provides low distortion and ground compatibility with low current consumption.

Figure 14: Typical Tone Response

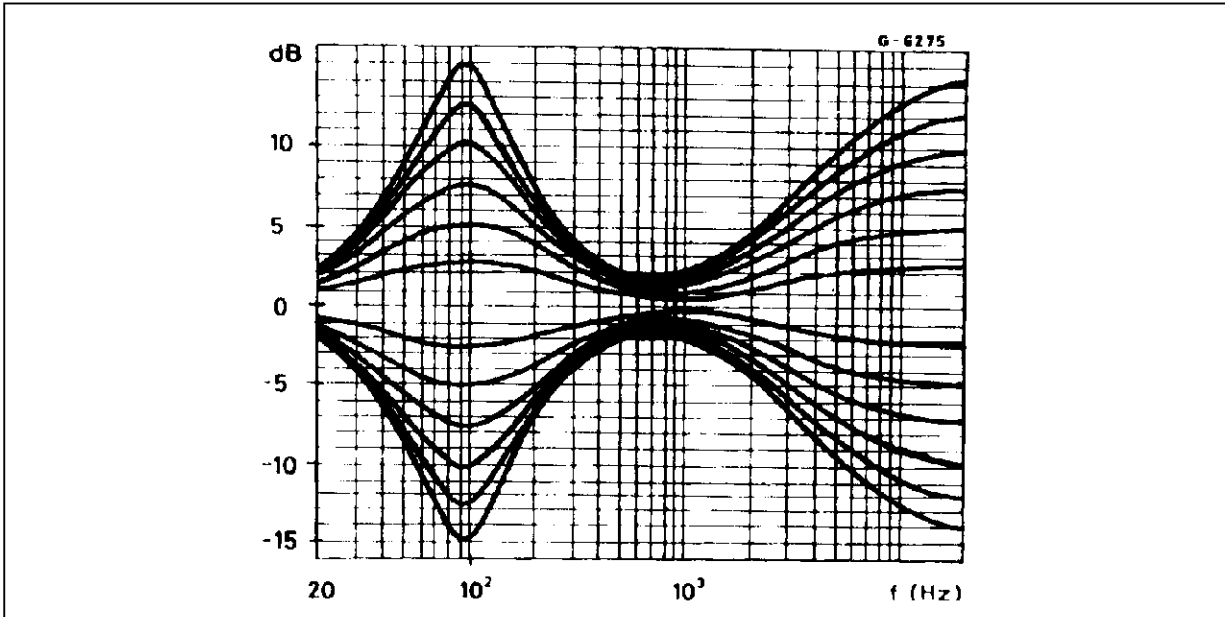
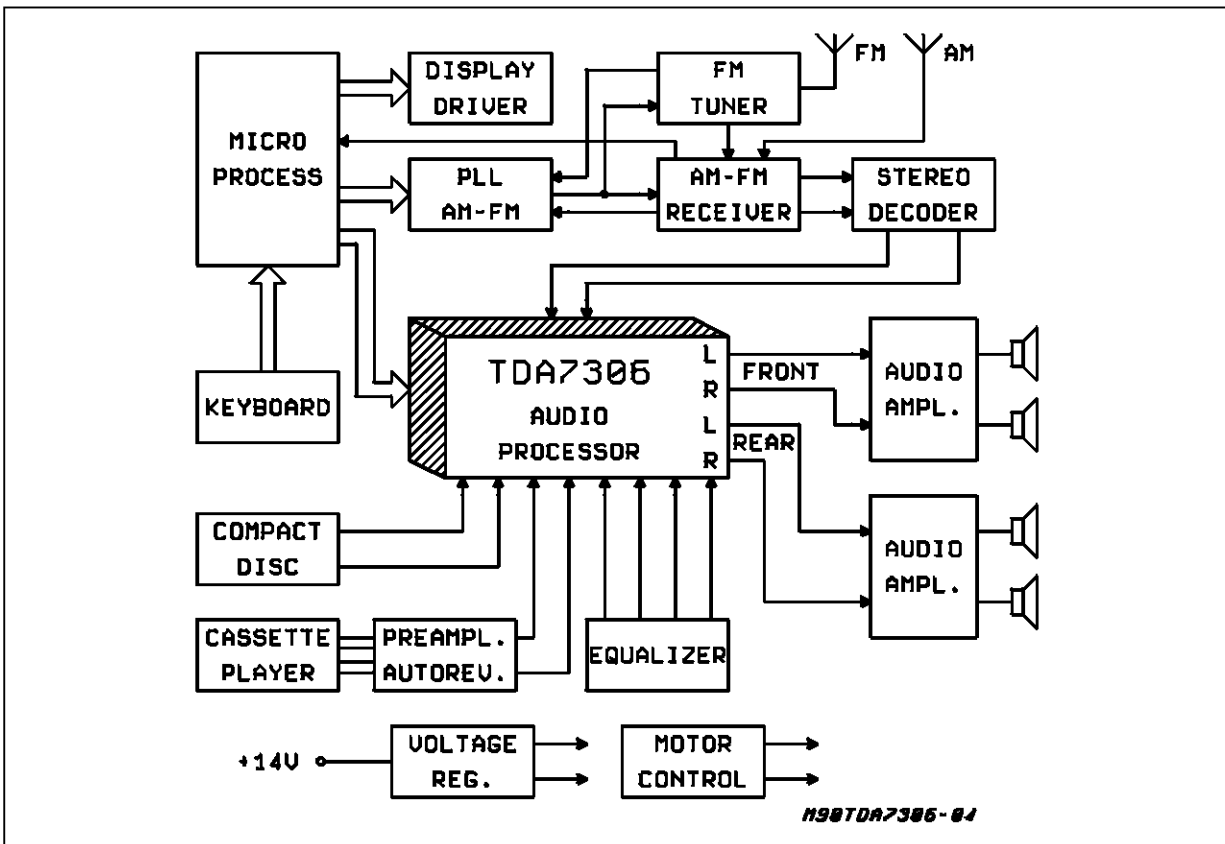


Figure 15: Complete Car-Radio System using Digital Controlled Audio Processor





**APPLICATION INFORMATION** (continued)**SERIAL BUS INTERFACE**

The serial bus interface is compatible to MICROWIRE and SPI bus systems.

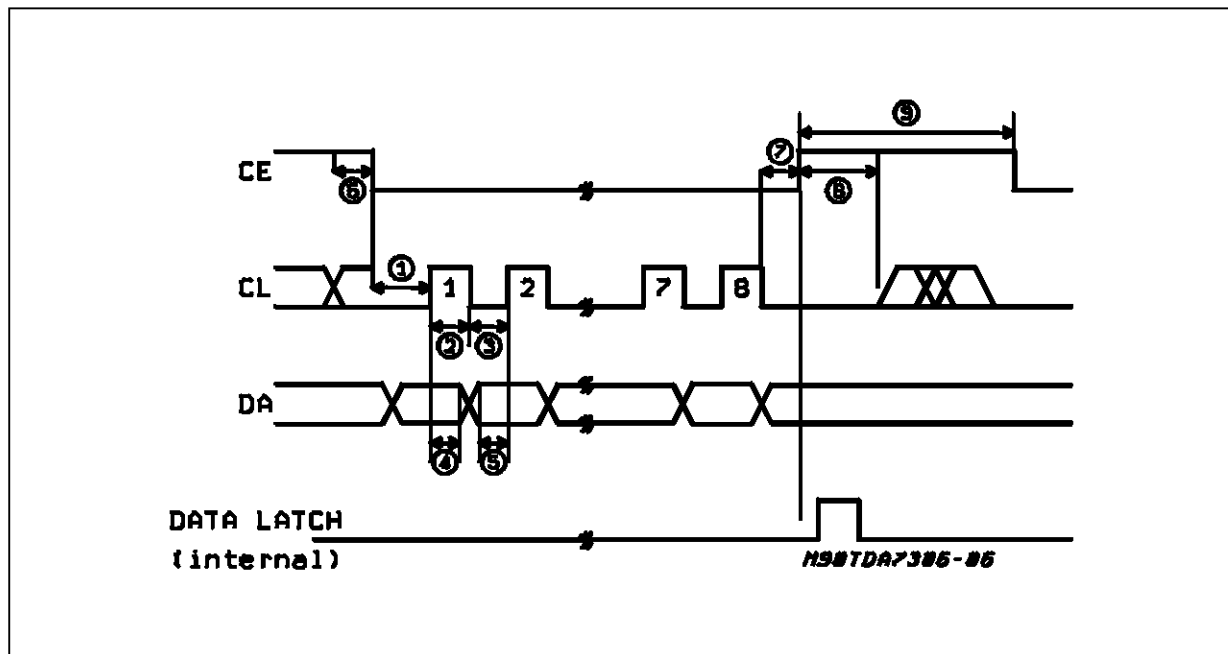
During the LOW state of the chip enable signal (CE) the data on pin DA are clocked into the shift register at the LOW to HIGH transition of the clock signal CL.

At the LOW to HIGH transition of the CE signal the content of the internal shift register is stored into the addressed latches.

The transmission is separated into bytes with 8 bit according to the data specification of the audio-processor. After every byte a positive slope of the CE signal has to be generated in order to store the data byte.

A special clock counter enables the latch of the data byte only, if exactly 8 clocks were present during the LOW state of the CE signal. This results in a high immunity against spikes on the clock line and avoids a storage of wrong databytes.

**Figure 16:** BUS Timing



Nr.	Parameter	Min.	Max.	Units
	Clock Frequency		250	KHz
1	CE Lead time	4		$\mu$ s
2	Clock High Time	2		$\mu$ s
3	Clock Low Time	2		$\mu$ s
4	Data Hold Time	1.8		$\mu$ s
5	Data Setup Time	1.8		$\mu$ s
6	Clock Setup Time	0		$\mu$ s
7	CE lagtime	0		$\mu$ s
8	Clock Hold Time	6		$\mu$ s
9	CE High Time	6		$\mu$ s

**SOFTWARE SPECIFICATION  
DATA BYTES**

MSB		LSB			Function			
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
0	1	0	X	X	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

**STATUS AFTER POWER-ON-RESET**

Volume	-66dB
Speaker	-38dB
Audio Switch	Mono
Bass	+2.5dB
Treble	+2.5dB

X = don't care Ax = 2dB steps Bx = 10dB steps  
Cx = 2.5dB steps

**VOLUME**

MSB		LSB				
0	0	B2	B1	B0	A2 A1 A0	Volume 2dB Steps
					0 0 0	0
					0 0 1	-1.6
					0 1 0	-3.2
					0 1 1	-4.8
					1 0 0	-6.4
					1 0 1	Not allowed
					1 1 0	Not allowed
					1 1 1	Not allowed
0	0	B2	B1	B0		Volume 10dB Steps
		0	0	0		+10
		0	0	1		+2
		0	1	0		-8
		0	1	1		-16
		1	0	0		-24
		1	0	1		-32
		1	1	0		-40
		1	1	1		-48

For example if you want setting the volume at -25.6dB the 8 bit string is: 0 0 1 0 0 0 0 1

**SPEAKER ATTENUATORS**

MSB		LSB				
1	0	0	B1	B0	A2 A1 A0	Speaker LF
1	0	1	B1	B0	A2 A1 A0	Speaker RF
1	1	0	B1	B0	A2 A1 A0	Speaker LR
1	1	1	B1	B0	A2 A1 A0	Speaker RR
					0 0 0	0
					0 0 1	-1
					0 1 0	-2
					0 1 1	-4
					1 0 0	-5
					1 0 1	Not allowed
					1 1 0	Not allowed
					1 1 1	Not allowed
		0	0			0
		0	1			-6
		1	0			-18
		1	1			-36

For example attenuation of 20dB on speaker RF is given by: 1 0 1 1 0 0 1 0

**SOFTWARE SPECIFICATION** (continued)

AUDIO SWITCH - Select the input Channel to Activate

MSB			LSB					
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Mute Input
			X	X	1	0	0	Mono
			X	X	1	0	1	Not Allowed
			X	X	1	1	0	Not Allowed
			X	X	1	1	1	Not Allowed

X = don't care

For example to set the stereo 2 channel the 8 bit string must be: 0 1 0 0 0 0 1

BASS AND TREBLE - Control Range of  $\pm 15$ dB (boost and cut) Steps of 2.5dB

0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	- 15
				0	0	0	1	- 15
				0	0	1	0	- 12.5
				0	0	1	1	- 10
				0	1	0	0	- 7.5
				0	1	0	1	- 5
				0	1	1	0	- 2.5
				0	1	1	1	- 0
				1	1	1	1	0
				1	1	1	0	2.5
				1	1	0	1	5
				1	1	0	0	7.5
				1	0	1	1	10
				1	0	1	0	12.5
				1	0	0	1	15
				1	0	0	0	15

C3 = Sign

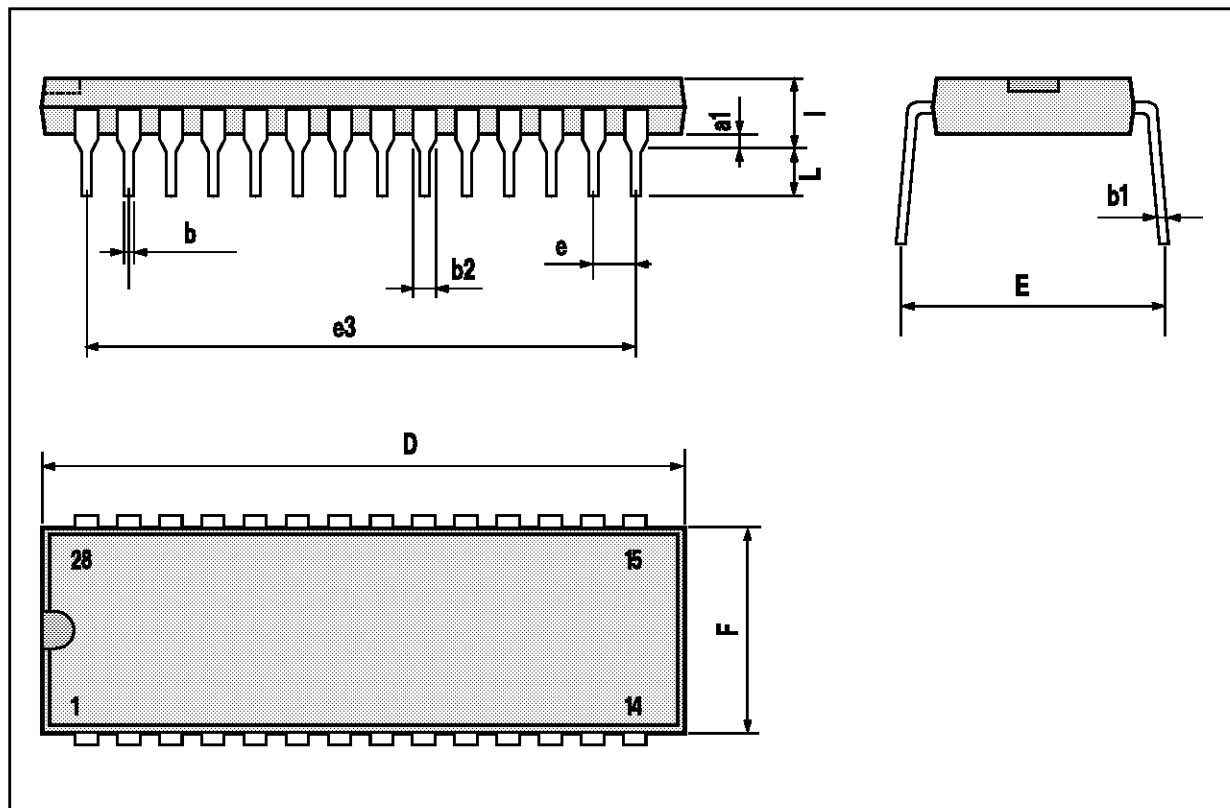
For example Bass at -12.5dB is obtained by the following 8 bit string: 0 1 1 0 0 0 1 0



# TDA7306

## DIP28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
l		4.445			0.175	
L		3.3			0.130	



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